



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/723,558	11/28/2000	Yotam Shefi	TI-30912	7897

23494 7590 06/07/2005

TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

EXAMINER

MARCELO, MELVIN C

ART UNIT PAPER NUMBER

2662

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/723,558

Applicant(s)

SHEFI ET AL

Examiner

Melvin Marcelo

Art Unit

2662

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 February 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6,7,9-11,23,24,26-28 and 36-43 is/are allowed.
- 6) ☒ Claim(s) 1-5,8,12-22,25 and 29-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 November 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

### **Response to Arguments**

1. Applicant's arguments filed 2-7-2005 have been fully considered but they are not persuasive. Schzukin et al. (US 6,694,388 B1) clearly teach a single queue assembled from three memory segment/blocks. See Figure 3 and column 7, lines 34-43.

### **Claim Rejections - 35 USC § 102**

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5, 8, 12-14, 18-20, 22, 25 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Schzukin et al. (US 6,694,388 B1).

Schzukin teaches the queue management system, wherein memory segments are called memory blocks. With respect to the claims below, references to the prior art appear in parenthesis.

1. *A method of queue management, said method comprising the steps of:*

*dividing a buffer memory into a plurality of memory segments, each memory segment comprising a plurality of bytes (Schzukin, queue memory divided into a plurality of blocks, each block comprising 64 entries, wherein 64 entries inherently would be greater than a single byte, column 6, lines 19-28);*

*constructing a plurality of queues, wherein at least one of said queues is assembled from two or more memory segments (Plurality of queues in column 6, lines 32-44 and a queue is assembled from three segment/blocks in Figure 3 and column 7, lines 34-43);*

*providing a write pointer and a read pointer for each queue (Column 7, lines 11-33 and 62-64); and*

*providing a plurality of next segment pointers, each next segment pointer associated with a different memory segment and adapted to indicate the next memory segment in a queue*

Art Unit: 2662

**(Pointers to the next memory block associated with entry 63 in the blocks shown in Figure 3 which form the linked list described in column 8, lines 13-19 and 43-50).**

2. *The method according to claim 1, further comprising the steps of: incrementing said write pointer when data is written to a queue; allocating an available memory segment when the current memory segment becomes full; and setting the next segment pointer associated with the current memory segment to point to the memory segment allocated to the queue (Column 8, lines 20-56).*

3. *The method according to claim 1, further comprising the step of providing a segment status table wherein an entry in said segment status table is adapted to indicate whether a corresponding memory segment is occupied or available for use in a queue (Empty list 60 in Figure 60, wherein each memory block is represented by an entry 62, column 6, lines 37-44).*

5. *The method according to claim 1, further comprising the step of flushing all queues simultaneously (Resetting the queue system flushes all queues simultaneously, column 52-58).*

8. *The method according to claim 1, further comprising the steps of: incrementing said read pointer when data is read from a queue; and setting said read pointer in accordance with the next segment pointer associated with the memory segment currently being read when the end of a memory segment is reached (Column 8, line 57 to column 9, line 30).*

12. *The method according to claim 1, further comprising providing an indication of the current size of each queue (Block Counter, column 7, lines 26-27).*

13. *The method according to claim 1, further comprising providing an indication of the combined total size of all queues (Empty counter 68 in Figure 2B provides an indication of the combined total size of all queues by counting the number of empty blocks left that can be shared by all queues, column 6, lines 45-51).*

14. *The method according to claim 1, further comprising the step of indicating when the size of a particular queue exceeds a user defined threshold (Column 8, lines 37-42).*

18. *A queue management system, comprising:*

*a buffer memory divided into a plurality of memory segments, each memory segment comprising a plurality of bytes (Schzukin, queue memory divided into a plurality of blocks, each block comprising 64 entries, wherein 64 entries inherently would be greater than a single byte, column 6, lines 19-28);*

*means for constructing a plurality of queues, wherein at least one of said queues is assembled from two or more memory segments (Plurality of queues in column 6, lines 32-44*

Art Unit: 2662

and a queue is assembled from three memory segment/blocks in Figure 3 and column 7, lines 34-43);

*a write pointer and a read pointer associated with each queue (Column 7, lines 11-33 and 62-64); and*

*a plurality of next segment pointers, each next segment pointer associated with a different memory segment and adapted to indicate the next memory segment in a queue (Pointers to the next memory block associated with entry 63 in the blocks shown in Figure 3 which form the linked list described in column 8, lines 13-19 and 43-50).*

19. *The system according to claim 18, further comprising: means for incrementing said write pointer when data is written to a queue; means for allocating an available memory segment when the current memory segment becomes full; and means for setting the next segment pointer associated with the current memory segment to point to the memory segment allocated to the queue (Column 8, lines 20-56).*

20. *The system according to claim 18, further comprising a segment status table wherein an entry in said segment status table is adapted to indicate whether a corresponding memory segment is occupied or available for use in a queue (Empty list 60 in Figure 60, wherein each memory block is represented by an entry 62, column 6, lines 37-44).*

22. *The system according to claim 18, further comprising means for flushing all queues simultaneously (Resetting the queue system flushes all queues simultaneously, column 52-58).*

25. *The system according to claim 18, further comprising: means for incrementing said read pointer when data is read from a queue; and means for setting said read pointer in accordance with the next segment pointer associated with the memory segment currently being read when the end of a memory segment is reached (Column 8, line 57 to column 9, line 30).*

29. *The system according to claim 18, further comprising indicating means adapted to indicate the current size of each queue (Block Counter, column 7, lines 26-27).*

30. *The system according to claim 18, further comprising indicating means adapted to indicate the combined total size of all queues (Empty counter 68 in Figure 2B provides an indication of the combined total size of all queues by counting the number of empty blocks left that can be shared by all queues, column 6, lines 45-51).*

31. *The system according to claim 18, further comprising means for indicating when the size of a particular queue exceeds a user defined threshold (Column 8, lines 37-42).*

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 15-17 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schzukin et al.

Schzukin does not explicitly set the number of memory segments or next segment pointers equal to 64, each memory segment comprising 64 bytes, the number of queues equals 9, nor a buffer memory comprising a dual ported memory. However, Schzukin explicitly suggests the above embodiments by stating “[o]ne skilled in the art may apply the principles of the present invention to construct a dynamic queue system having a size, number of memory blocks, and memory block size in accordance with the requirements of the particular application” (column 6, lines 60-64), wherein Schzukin’s disclosed number of memory blocks with its associated next segment pointers (entry63) equals 127, each memory block comprises 64 entries and the number of queues is one or more is an example provided for illustration purposes only (column 6, lines 59-60). Further, Schzukin states that “[t]he queue memory may be constructed using any suitable read/write memory such as random access memory (RAM), non volatile RAM (NVRAM), or other types of memory” (column 6, lines 28-31). A skilled artisan would have been motivated by Schzukin’s statements to recognize that the number of memory segments and next segment pointers, memory segment size, number of queues and type of buffer memory are design choices based on the particular application to be used. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the particular claimed embodiments since Schzukin explicitly suggests that these features are design choices.

Art Unit: 2662

- 15. *The method according to claim 1, wherein the number of memory segments and next segment pointers equals 64.*
- 16. *The method according to claim 1, wherein each memory segment comprises 64 bytes.*
- 17. *The method according to claim 1, wherein the number of queues equals 9.*
- 32. *The system according to claim 18, wherein the number of memory segments and next segment pointers equals 64.*
- 33. *The system according to claim 18, each memory segment comprises 64 bytes.*
- 34. *The system according to claim 18, wherein the number of queues equals 9.*
- 35. *The system according to claim 18, wherein said buffer memory comprises a dual ported memory.*

6. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schzukin et al. in view of Jones (US 6,590,901 B1).

Schzukin does not teach flushing each queue separately. However, Jones teaches to provide a "flush queue" command to a specified queue for the purpose of responding to serious unexpected events, such as failure of a network interface (column 15, lines 37-43). Therefore, it would have been obvious to be able to flush each queue separately since a skilled artisan would have been motivated to provide a "flush queue" command in order to respond to network interface failures as taught by Jones.

- 4. *The method according to claim 1, further comprising the step of flushing each queue separately.*
- 21. *The system according to claim 18, further comprising means for flushing each queue separately.*

**Allowable Subject Matter**

7. Claims 6, 7, 9-11, 23, 24, 26-28 and 36-43 are allowed.

**Conclusion**

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


Art Unit: 2662

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Marcelo whose telephone number is 571-272-3125. The examiner can normally be reached on Mon-Fri 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Melvin Marcelo  
Primary Examiner  
Art Unit 2662

June 2, 2005